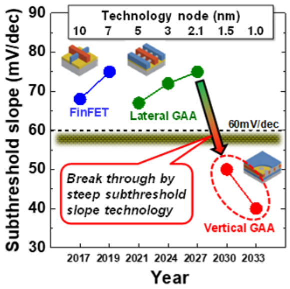
R-DIBL and NDR Caused by Transient Negative Capacitance and The Impact of Charge Trap in FeFET

強誘電体トランジスタにおける負性容量による逆DIBLと負性抵抗の発現，および電荷トラップの影響

Background



The need for steep slope transistor to breakthrough the physical limit

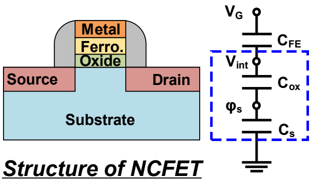
Advantages of NCFET

- High on-state current
- CMOS compatible material (FE-HfO$_2$) and process
- Minimum circuit design modification

Subthreshold slope (SS):

$$SS=\frac{\partial V_G}{\partial(\log_{10} I_D)}=\frac{\partial \varphi_s}{\partial(\log_{10} I_D)}\frac{\partial V_G}{\partial \varphi_s}=60\frac{\partial V_G}{\partial V_{int}}\frac{\partial V_{int}}{\partial \varphi_s}=60\left(1+\frac{C_{int}}{C_{FE}}\right)\left(1+\frac{C_S}{C_{OX}}\right)$$

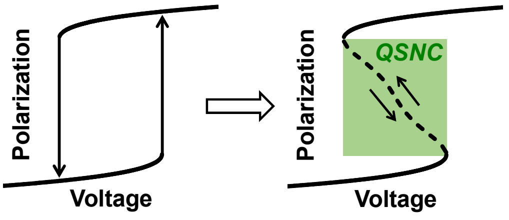
Negative C_{FE} → <1 → Sub-60 mV/dec SS



Structure of NCFET

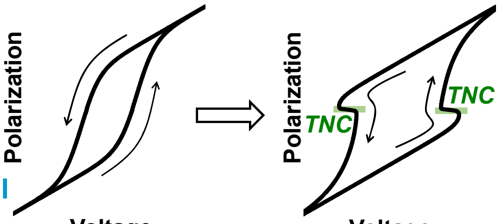
NC effect: Static vs Transient

Quasi-static NC (QSNC) predicted by single-domain Landau theory



P-V of Standalone FE ***P-V of FE-DE***

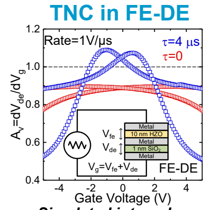
Transient NC (TNC) with multi-domain Preisach model



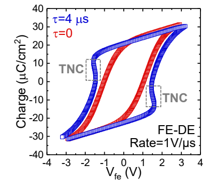
P-V of FE in static condition ***Transient condition***

Transient NC and related physics

TNC in FE-DE

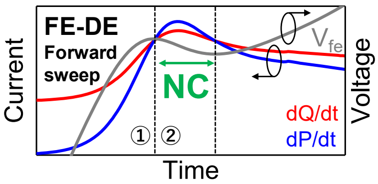


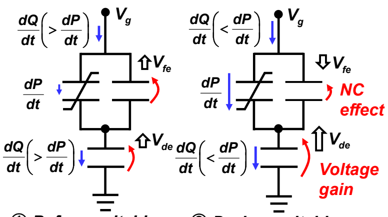
Simulated internal voltage amplification



Simulated Q-V of FE

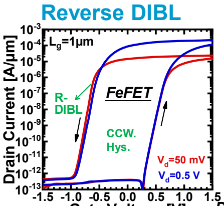
Mechanism of TNC

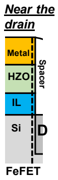




① Before switching ② During switching

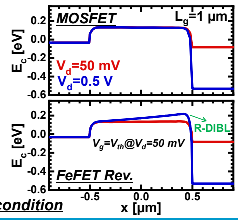
Reverse DIBL





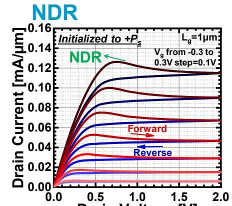
R-DIBL

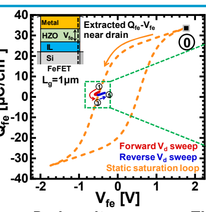
- $V_d=V_{high}$ or V_{low}
- V_{high} → high V_{ch}
- Low $|Q_{ch}|$ at fixed V_g
- $Q_{fe}=|Q_{ch}|$ → low Q_{fe}
- High V_{fe} (TNC)
- Lower voltage across IL and Si
- Lower $|Q_{ch}|$ & I_d → R-DIBL

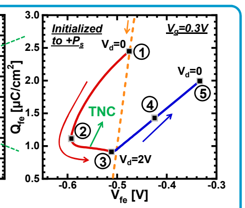


Drain coupling modifies TNC condition

NDR



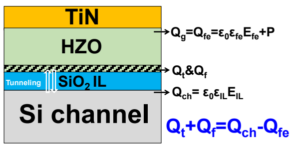




Drain voltage causes TNC just as gate voltage does.

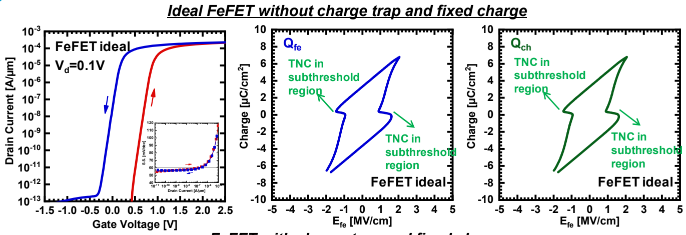
Impact of charge trap & fixed charge

MFIS with charge trap & fixed charge

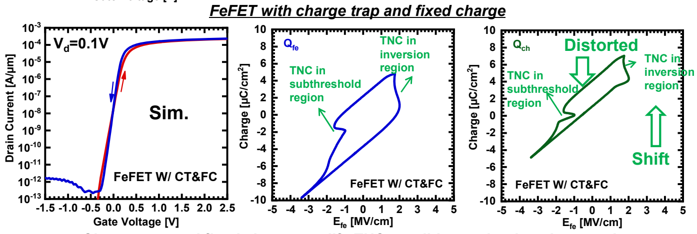


- It is inevitable to form charge trap and fixed charge in MFIS structure.
- A sheet with traps and fixed charge are assumed at the bottom of HZO.
- N_t is 2.6×10^{20}cm^{-3} and the traps are uniformly distributed 0.83eV above the midgap with a bandwidth of 0.22eV.
- N_f is assumed to be 3×10^{13}cm^{-2}.

Ideal FeFET without charge trap and fixed charge

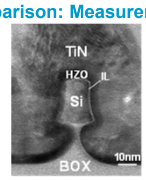


FeFET with charge trap and fixed charge

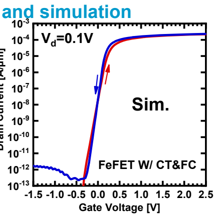


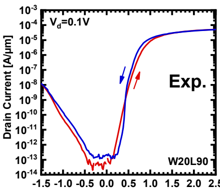
Charge trap and fixed charge modify TNC condition and reduce hysteresis.

Comparison: Measurement and simulation



Good agreement of hysteresis-free and sub 60mV/dec SS.





Summary

1) Develop simulation framework for FeFET based on the TNC theory and explore the physical mechanism of TNC.
2) The model clarified the mechanism of R-DIBL and NDR which are uniquely observed in FeFET.
3) Charge trap and fixed charge are incorporated in the model and reproduced measurement result of hysteresis-free and steep SS FeFET.

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